High-Throughput LabVIEW FPGA

Overview
The High-Throughput LabVIEW FPGA course teaches you the essential skills and processes to become proficient at designing high-performance applications with LabVIEW FPGA. During this course, learn about FPGA hardware resources and how LabVIEW code maps to these resources. Review case studies, architectural considerations, and simulations to learn NI recommended design flow when implementing large FPGA applications.

NOTE: National Instruments offers two courses over the LabVIEW FPGA module. The class most appropriate for you depends on the hardware and I/O rate of your application. Review the descriptions below to determine if the High-Throughput LabVIEW FPGA course or the LabVIEW FPGA course is right for you:

- **High-Throughput LabVIEW FPGA**: This course focuses on new FPGA hardware targets with extremely high-performance I/O coupled with real-time and low-latency FPGA-based processing such as NI FlexRIO. This course teaches programming practices like single-cycle timed loop which are essential when programming LabVIEW FPGA for I/O rates higher than 5 MHz.
- **LabVIEW FPGA**: This course focuses on programming practices for applications with I/O less than 5 MHz or using R Series, CompactRIO, or Single-Board RIO targets.

Duration
Classroom: 3 Days

Audience
- Anyone considering developing applications using NI-RIO devices with high I/O rates (>5 MHz, e.g. NI FlexRIO hardware) and requiring customization through LabVIEW FPGA

Prerequisites
- LabVIEW Core 1 course or equivalent experience
- Familiarity with FPGA development using LabVIEW FPGA or otherwise is helpful, but not required
- Familiarity with FPGA targets in the LabVIEW project and environment is helpful, but not required

NI Products Used During the Course
- LabVIEW Professional Development System Version 2011 or later
- LabVIEW FPGA Module Version 2011 or later
- LabVIEW Digital Filter Design Toolkit
- NI-RIO device driver
- NI FlexRIO FPGA and adapter modules

After attending this course, you will be able to:
- Understand how LabVIEW VIs are compiled for FPGA targets
- Develop applications on top of the NI-RIO device driver
- Develop high-performance DSP algorithms and digital designs in LabVIEW for FPGAs
- Integrate existing code (both LabVIEW and HDL) into LabVIEW FPGA applications

Registration
Register online at ni.com/training or call (800) 433-3488 Fax: (512) 683-9300 email info@ni.com

Outside North America, contact your local NI Office.
Worldwide Contact Info: ni.com/global

Part Number
910820-xx
-01 NI Corporate or Branch
-11 Regional
-21 Onsite (at your facility)
High-Throughput LabVIEW FPGA Course Outline

- Architect high-performance FPGA-based systems
- Follow NI-recommended development and debug processes for efficient FPGA implementation

Suggested Next Courses
- NI FlexRIO

Day 1

Graphical Design in LabVIEW FPGA
The goal of this section is to provide insight into FPGA hardware resources, and how LabVIEW code maps to these resources in terms of size and propagation delay/loop rate. Topics include:
- Introduction to FPGAs
- Mapping LabVIEW primitives to FPGA resources
- Execution time/propagation delay/critical path/loop rate/clock rate
- Throughput

Host Communication with LabVIEW FPGA through NI-RIO
This lesson covers the methods of interacting between host and FPGA VIs. Topics include:
- Memory-mapped register access
- DMA
- Interrupts
- Interactive and programmatic FPGA VI execution

I/O in LabVIEW FPGA
There are many methods of connecting the LabVIEW FPGA VI to other logic on the FPGA as well as I/O outside the FPGA. Topics include:
- User CLIP
- Socketed CLIP
- Importing HDL into CLIP
- Target I/O
- Synchronous and asynchronous I/O

- Metastability and glitching, synchronization registers

Day 2

Crossing FPGA Clock Domains
Large applications often involve logic running at multiple rates. There are specific considerations for exchanging data between these “clock domains.” Topics include:
- Use cases for multiple clock domains
- Global and Local Variables
- Handshaking
- FIFOs
- 2 and 4-wire handshaking introduction
- Memory items

LabVIEW FPGA Algorithm Design - DSP Case Study
To illustrate the NI recommended design flow, this lesson presents a case study on DSP design. Topics include:
- Recommended FPGA design flow
- FIR filter introduction
- Behavioral and structural models
- IP sources
- Fixed-point math
- Test benches
- Dataflow-accurate FPGA simulation
- Algorithm implementation options
- Balancing performance and portability
- Integrating IP with the IP Integration Node
- Comparison of the IP Integration Node and the CLIP Node
- Xilinx IP palette
- Hardware test

LabVIEW FPGA Algorithm Design - Digital Protocol Case Study
To illustrate the NI recommended design flow, this lesson presents a case study on digital protocol implementation. Topics include:
- Recommended FPGA design flow
- State machine theory
- State machines in LabVIEW
High-Throughput LabVIEW FPGA Course Outline

- State machine execution timing
- SPI protocol introduction
- Test benches
- Dataflow-accurate FPGA simulation
- Hardware test
- Digital Debouncing
- Bit Error Rate Test (BERT)
- FPGA resets

Day 3
LabVIEW FPGA Architectures
There are additional architectural considerations when building large FPGA applications. This section covers a design from concept to implementation. Topics include:

- Concept to Implementation design flow
- Throughput requirements
- Storage requirements
- Clocking architecture
- Communication policies
- Case study on an FPGA-based multi-record averager and FFT
- Best practices for large FPGA designs

Simulation and Debug of FPGA Designs with Third-Party Tools
While most designs can be simulated with sufficient fidelity in LabVIEW, for completely bit-true, cycle accurate simulation, some designs may require a third-party cycle-accurate simulator. Topics in this section include:

- Overview of cycle-accurate simulation
- Simulation in Mentor Graphics ModelSim and Xilinx Isim
- VHDL test benches
- Co-simulation with LabVIEW